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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/062,650	01/31/2002	Neil Robert McLellan	36080.01101	7196

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EXAMINER

LUU, CHUONG A

ART UNIT PAPER NUMBER

2825

DATE MAILED: 07/22/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/062,650

Applicant(s)

MCLELLAN ET AL.

Examiner

Chuong A Luu

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-38 is/are pending in the application.
- 4a) Of the above claim(s) 23-38 is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-22 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on ____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 5.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). ____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Inventorship

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Election/Restrictions

Restriction to one of the following inventions is required under 35 U.S.C. 121:

- I. Claims 1-22, drawn to a method of fabrication of a semiconductor device, classified in class 438, subclass 197.
- II. Claims 23-38, drawn to a semiconductor device, classified in class 257, subclass 666+.

Inventions Group I and Group II are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different

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process (MPEP § 806.05(f)). In the instant case, encapsulating can be substituted by underfilling process.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification and because these inventions are distinct for the reasons given above and the search required for Group I is not required for Group II, restriction for examination purposes as indicated is proper, restriction for examination purposes as indicated is proper.

During a telephone conversation with Mr. Christopher J. Gasper on June 24, 2003 a provisional election was made because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)) to prosecute the invention of Group I, claims 1-22. Affirmation of this election must be made by applicant in replying to this Office action. Claims 23-38 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

PRIOR ART REJECTIONS

Statutory Basis

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The Rejections

Claims 1-3, 6-9, 11-14 and 18-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Shin et al. (U.S. 6,395,578 B1).

Shin discloses a method for fabricating a semiconductor package with

(1); (19) providing a substrate (11) comprising:

a first surface (11a),

a second surface (11b) opposite said first surface (11a),

a cavity through said substrate between said first and second surfaces,

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a conductive via extending through said substrate and electrically connecting said first surface of said substrate with said second surface of said substrate;

applying a closure member (70) (a strip) to said second surface of said substrate);

mounting a semiconductor die (30) on said closure member (70) (a strip), at least a portion of said semiconductor die (30) being disposed inside said cavity;

encapsulating (50) in a molding material at least a portion of said first surface (11a) of said substrate (11);

removing said a closure member (70) (a strip) from said substrate (11) (see Figure 7A-7E);

(2) said encapsulating further comprising filling said cavity with said molding material, wherein a surface of said semiconductor die is exposed to said strip (see Figure 7D);

(3) further comprising attaching a thermal element to said exposed surface of said semiconductor die (see Figure 7E);

(6) said mounting said semiconductor die comprising disposing said die in its entirety inside said cavity (see Figure 7A-7E);

(7) said thermal element comprising a copper heat slug (see column 9, lines 30-35);

(8) said substrate further comprising a multi-layer circuit trace (see Figure 7A-7E);

(9) further comprising, after said mounting said semiconductor die on said strip, interconnecting said semiconductor die to a first trace embedded in said first surface of said substrate (see Figure 7A-7E);

(11) said encapsulating comprising a liquid molding process (see column 7, lines 9-11);

(12) said encapsulating comprising a transfer molding process (see column 7, lines 5-9);

(13) said encapsulating comprising encapsulating said first surface of said substrate in its entirety (see Figure 7D);

(14) further comprising attaching a solder element to a second trace embedded in said second surface of said substrate (see Figure 7E);

(18) said applying said strip further comprising sealing a portion of said cavity (see Figure 7B);

(20) further comprising singulating said substrate into a plurality of integrated circuit packages (see Figure 7F);

(21) said singulating comprising a sawing process (see column 10, lines 22-24).

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Claims 4-5, 15-17 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shin et al. (U.S. 6,395,578 B1) in view of Juskey et al. (U.S. 6,507,102 B2)

Shin teaches the above outlined features except for said attaching said thermal element comprising bonding a thermally conductive adhesive to said thermal element; a punching process.. However, Juskey discloses a semiconductor structure with **(4)** said attaching said thermal element comprising bonding a thermally conductive adhesive to said thermal element; **(5)** said attaching said thermal element further comprising attaching said thermal element to said second surface of said substrate (see column 7, lines 32-55. Figure 5); **(15)** said applying said strip comprising applying an adhesive material on at least a portion of said strip to said second surface of said substrate (see Figure 5); **(16)** said strip comprising a high temperature stable polyimide (see column 4, lines 10-37); **(17)** said mounting said semiconductor die comprising attaching said semiconductor die to said adhesive material on said strip (see Figure 5); **(22)** said singulating comprising a punching process (see columns 4 and 5, lines 53-54 and lines 54-56, respectively). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the above teachings by applying adhesive to the heat sink which can be selected with a polyimide material during fabrication a

semiconductor device to exceed its performance criteria. (Please notice Shin Col. 9, lines 29-37, tape, and a copper sheet may comprise member 70; Juskey discloses polyimide as a material for the strip, so that one of ordinary skill in the art would be motivated to use polyimide for the same purpose in the method taught by Shin.)

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shin et al. (U.S. 6,395,578 B1) in view of Combs (U.S. 5,596,231).

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Shin teaches everything above except for said interconnecting comprising a thereto-sonic wire bonding process. However, Combs discloses a semiconductor package with **(10)** said interconnecting comprising a thereto-sonic wire bonding process (see column 6, lines 53-60). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Shin and Combs by applying thereto-sonic wire bonding process to fabricate a semiconductor device to exceed its performance criteria.

Conclusion


The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuong A Luu whose telephone number is (703)305-0129. The examiner can normally be reached on M-F (7:30-4:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (703)308-1323. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7722 for regular communications and (703)308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.


CHAD EVERETT
PRIMARY EXAMINER


CAL
July 11, 2003